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EXAMINER	
FONG, VINCENT	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/537,742	BEHLING ET AL.	
	Examiner	Art Unit	
	Vincent Fong	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 June 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06-03-2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed on 06-03-2005.

Claims 1-10 are pending and have been examined.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement filed 06-03-2005 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Drawings

3. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: element v. a (page 6 line 29) and element vi. b (page 6 line 30). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.

(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

5. The disclosure is objected to because of the following informalities:

The word "than" (page 6 line 23) should be replaced by "then".

Appropriate correction is required.

6. Claims 1, 2, 3, 5, 6, 7 and 10 are objected to because of the following informalities:

As per claim 1, the terms "the data transfer" and "the registers" lack antecedent basis, they should be changed to "data transfer" and "register data value" respectively and will be treat as such for examination. In addition, the reference character 40 for arithmetic unit should be deleted.

As per claim 2, the terms "the memory" and "the registers" lack antecedent basis, they should be changed to "the peripheral memory" and "registers data value" respectively

and will be treat as such for examination. In addition the meaning of the term "which set of registers" is unclear, it should be change to "in which the set of registers" and will be treat as such in the examination.

As per claim 3, the term "the memory", "the start address" and "the data" lack antecedent basis, they should be changed to "the peripheral memory", "start address" and "data" respectively and will be treat as such for examination.

As per claim 5, the term "the register sets" lack antecedent basis, it should be changed to "register data value sets" and will be treat as such for examination.

As per claim 6, the terms "the set of temporary registers" and "the set of main register" lack antecedent basis, they should be changed to "set of temporary registers" and "set of main register" respectively and will be treat as such for examination.

As per claim 7, the term "the control register" lacks antecedent basis, it should be changed to "control register" and will be treat as such for examination.

As per claim 10, the term "the start address" lack antecedent basis, it should be changed to "start address" and will be treat as such for examination. The terms "the set of temporary registers is complete" and "the set of temporary registers is incomplete " are unclear, they should be changed to "the set of temporary registers is filled" and "the set of temporary registers is not filled" and will be treat as such in examination. In addition the reference characters (+) and (-) should be deleted.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 10 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The method as claimed includes a conditional statement (v.b) if the set of temporary registers is incomplete, proceeding to method step (iii), if the set of temporary keep remaining not filled, the method would not proceed to the other branch of the conditional statement; and ultimately proceed to step (ix). In such case the method will not produce a useful, concrete and tangible result as such result is create in step (ix) starting of the calculation in the arithmetic unit, and in this case the method will not reach the step (ix). In addition the claim includes a conditional statement (vi.a) if the arithmetic unit is active, proceeding to method step (vi), if the arithmetic unit keep remaining active, the method would not proceed to the other branch of the conditional statement; namely proceed to step (vii) through step (vi. b). In such case the method will not produce a useful, concrete and tangible result as such result is create in step (ix) starting of the calculation in the arithmetic unit, and in this case the method will not reach the step (ix).

Examiner suggest that changing the conditional statement of "if..." to "in response to..." to avoid the deficiency created by the use of conditional statements in claim 10.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 1-9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Regarding claim 1, the phrase "for example" renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d). For examination the limitation following the phrase "for example" are not consider part of the claimed invention.

11. As per claim 6, the phrase "one set of registers" renders the claim indefinite, because it is not clear whether the limitation is referring to the set of main registers or set of temporary registers or both. For examination the phrase is treated as meaning "any one group of registers".

12. Any claim not specifically addressed above, is being rejected as incorporating the deficiencies of a claim upon which it depends.

Double Patenting

13. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir.

1985); *In re Van Omum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

14. Claims 1, 3, 4 and 8-9 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 2 and 4 of U.S. Patent No.5889622 in view of official notice. Although the conflicting claims are not identical, they are not patentably distinct from each other.

As per claim 1, the patented claim 1 discloses:

at least one microprocessor (line 2) and having at least one additional arithmetic unit (line 3) for performing at least one particular defined calculation (lines 3-4), the arithmetic unit being coupled to the microprocessor via a number of registers [couple via a number of first and second registers (lines 2-4)], of which first registers are provided for controlling the data transfer (line 5) and second register are provided to transmitting commands [transfer of instruction (lines 7-8)].

The patented claim 1 does not disclose that the register data value may be loaded from at least one particularly peripheral memory.

However, examiner takes official notice that register data value may be loaded from at least one particular peripheral memory is common in the art. Therefore it would be obvious to ordinary skill in the art at the time of invention to do so, ordinary skill in the

art would be motivated to let the user can store the program on a non volatile storage and enable the processing device make use of the program.

As per claim 3, rejection of claim 1 is incorporated and the patented claim 2 discloses: memory may be acted upon by at least one address register intended for pointing to the start address of the data to be loaded (address of the operands)(lines 2-4)[and the address of the data is inherently loading from some kind of memory], which the address register is connected to at least on control logic circuit (microprocessor).

As per claim 4, rejection of claim 3 is incorporated and the patented claim 2 discloses: A arithmetic unit (claim 1 line 3) which inherent has a control register and the arithmetic unit is connected to the microprocessor (claim 1 lines 4-5) thus the control register is connected to the control logic circuit (microprocessor claim 1 line 2).

As per claim 8, rejection of claim 1 is incorporated and the patented claim 4 discloses: A portable data carrier having at least one data processing device as claimed in instant claim 1 (lines 1-2).

As per claim 9, rejection of claim 1 is incorporated and the patented claim 4 discloses: The data processing device as claimed in instant claim 1.
The patented claim 1 does not disclose a semiconductor chip that comprises at least one of the data processing device.

However, examiner takes official notice that implementing the portable data carrier in semiconductor chip is common in the art. Therefore it would be obvious to ordinary skill in the art at the time of invention to do so, ordinary skill in the art would be motivated to take advantage of the lower power consumption and higher speed of semiconductor when in comparison with the older technology.

15. Claims 2 and 6-7 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No.5889622 in view of official notice, further in view of Blount et al. (WO 97/34226, hereinafter Blount). Although the conflicting claims are not identical, they are not patentably distinct from each other.

As per claim 2, rejection of claim 1 is incorporated and the patented claim 1 discloses: A arithmetic unit (line 3) which inherently having a set of main registers assigned to and intented for storing data value for active calculation and registers are assigned [being able to load data from memory] to memory (see double patenting rejection for claim 1). Patented claim 1 does not disclose one set of temporary registers connected to a set of main registers.

However Blount discloses a set of temporary registers (Blount AAH, ABH figure 6) connected to main register (Blount element 35 figure 6) and for storage of data for the active calculation in the ALU [the data in the register represents the input of the

MAC/ALU (Blount page 11 paragraph 4)] for the purpose of sharing instruction words between adjacent processors (Blount page 11 paragraph 4).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have multiple temporary registers connected to the set of main registers in the system of patented claim 1 because Blount teaches that the multiple temporary registers enable instruction data to be shared between adjacent processor (Blount page 11 paragraph 2). Enable instruction data to be shared between adjacent processor [the microprocessor and the arithmetic unit] will enable the sharing of workload.

As per claim 6, rejection of claim 1 is incorporated and patented claim 1 discloses:

A arithmetic unit (line 3) which inherently having a set of main registers and a microprocessor (line 2) which inherently has a set of registers assigned.

Patent claim 1 does not discloses the selection circuit and the set of temporary registers.

However Blount discloses at least one set of temporary registers (AAH, ABH figure 6) and at least one selection circuit (element 34 figure 6) is connect between temporary and main register for the purpose of sharing instruction words between adjacent processors (Blount page 11 paragraph 4).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have multiple temporary registers connected to the set of main registers in the system of patented claim 1 because Blount teaches that the multiple temporary registers enable instruction data to be shared between adjacent processor (Blount page

11 paragraph 2). Enable instruction data to be shared between adjacent processor [the microprocessor and the arithmetic unit] will enable the sharing of workload.

As per claim 7, rejection of claim 6 is incorporated and patented claim 1 discloses: control register (first and second register lines 5-8).

Patented claim 1 does not disclose that selection circuit may be acted upon by at least one bit position of the control register.

Blount discloses the selection circuit (element 34 figure 6) may be acted upon by at least one bit position of the control register (element 2 figure 1) (page 5 paragraph 7) [the control register control what is executed on the processor (table 1) thus control what data does the selection circuit select for processing in the ALU].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have selection circuit to act upon by a bit of control register to select which register to use for calculation in the system of patented claim 1 because Blount teaches that selecting register value from different sources enable instruction data to be shared between adjacent processor (Blount page 11 paragraph 2). Enable instruction data to be shared between adjacent processor [the microprocessor and the arithmetic unit] will enable the sharing of workload.

16. Claim 5 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent No.5889622 in view of

official notice, further in view of Hooker (USPN 6832296). Although the conflicting claims are not identical, they are not patentably distinct from each other.

As per claim 5, rejection of claim 3 is incorporated and patented claim 2 discloses the instant claim 3.

Patented claim 2 does not disclose a count register.

However Hooker discloses a counting register (element 124 figure 1) for indicating the register sets [data in cache line] to be loaded in sequence [incrementing by cache line size each fetch (element 532 figure 1, column 10)] is assigned to the control logic circuit (element 144 figure 1) to indicate the amount of data to be fetched into the cache.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the system of patented claim 2 to include a counting register to specify the amount of data left to fetch (Hooker column 2 line 67 – column 3 line 1). By indicating the amount of data left to fetch, repeated loading of the register for controlling data transfer could be avoided.

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

18. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Wille et al. (USPN 5889622, hereinafter Wille).

Wille discloses a data processing device (element 1 figure 1) having at least one microprocessor (element 2 figure 1) and having at least one additional arithmetic unit (element 3 figure 1) for performing at least one particular defined calculation, the arithmetic unit being coupled to the microprocessor via a number of registers (element 10 and 14-17 figure1) [the microprocessor is coupled to the arithmetic unit via further register (Column 2 lines 26-29), also the microprocessor is coupled to arithmetic unit via operand, result register (element 14-17 figure 1) and read/write memory (element 6 figure 1) by the exchange of data at the memory (column 2 lines 39-42)], of which first registers (element 211, 221 figure 2) are provided for controlling the data transfer [they control the location of operands to be loads (column 3 lines 28-31)] and second registers (element 201,202, 203 figure 2) are provided for transmitting commands [they contain the operation code which specify the command (column 3 lines 24-26)], characterized in that register data value may be loaded [the operand value for the instruction is loaded from non volatile memory and the memory (column 2 lines 33-37)] from at least one particularly peripheral memory (element 4, 6 figure 1).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

21. Claim 2,3,4,6,7,8,9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wille in view of Blount et al. (WO 97/34226, hereinafter Blount).

As per claim 2, the rejection of claim 1 is incorporated and Wille further discloses:
A temporary register (element 12 figure 1) is assigned to the memory (element 4 figure 1) [the temporary register is at the output of memory and only takes input from the memory (column 2 lines 52-54)], in which the register (element 12 figure 1) is connected to at least one set of main registers (element 14-16 figure 1) assigned to the arithmetic unit (element 3 figure 1) and intended for storage of registers data value for the active calculation [the set of main registers is responsible for storing the operands which is the data part of the instruction (Column 2 lines 33-34)].
Wille does not disclose at least one set of temporary registers.
However Blount discloses a set of temporary registers (Blount AAH, ABH figure 6) connected to main register (Blount element 35 figure 6) and for storage of data for the active calculation in the ALU [the data in the register represents the input of the

MAC/ALU (Blount page 11 paragraph 4)] for the purpose of sharing instruction words between adjacent processors (Blount page 11 paragraph 4).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have multiple temporary registers connected to the set of main registers in the system of Wille because Blount teaches that the multiple temporary registers enable instruction data to be shared between adjacent processor (Blount page 11 paragraph 2). Enable instruction data to be shared between adjacent processor [the microprocessor (Wille element 5 figure 1) and the arithmetic unit (Wille element 3 figure 1)] would not have to go through the memory (Wille element 6 figure 1) thus the reduction of time need for exchanging data between the microprocessor and the arithmetic unit.

As per claim 3, the rejection of claim 1 is incorporated and Wille further discloses: the memory (element 5 or 6 figure 1) may be acted upon by at least one address register intended for pointing to the start address of the data to be loaded (element 211 or 221 figure 2) [the starting address for loading operands (column 3 lines 28-31)], which address register is connected to at least one control logic circuit (element 29 figure 2) [to control what is send to the arithmetic unit (column 3 lines 4-7)].

As per claim 4, the rejection of claim 3 is incorporated and Wille further discloses: device characterized in that assigned to the arithmetic unit is at least one control register (element 201 figure 31) [the register control what is select by the selection

circuit (column 3 lines 4-8)], which is connected to the control logic circuit (element 29 figure 2).

As per claim 6, the rejection of claim 1 is incorporated and Wille further discloses:
A temporary register (element 12 figure 1) and the set of main registers (element 14-16 figure 1) connected and at least one set of registers assigned to the microprocessor [main registers receive data from memory (element 6 figure 1) (column 2 lines 33-37) and memory can be accessed by microprocessor (column 2 lines 39-42) thus the microprocessor can be passing data to the main registers through memory].
Wille does not disclose at least one set of temporary registers and at least one selection circuit is connected between temporary and main registers.
However Blount discloses at least one set of temporary registers (AAH, ABH figure 6) and at least one selection circuit (element 34 figure 6) is connect between temporary and main register for the purpose of sharing instruction words between adjacent processors (Blount page 11 paragraph 4).
It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have multiple temporary registers connected to the set of main registers in the system of Wille because Blount teaches that the multiple temporary registers enable instruction data to be shared between adjacent processor (Blount page 11 paragraph 2). Enable instruction data to be shared between adjacent processor [the microprocessor (Wille element 5 figure 1) and the arithmetic unit (Wille element 3 figure 1)] would not have to go through the memory (Wille element 6 figure 1) thus the

reduction of time need for exchanging data between the microprocessor and the arithmetic unit.

As per claim 7, the rejection of claim 6 is incorporated and Blount further discloses: the selection circuit (element 34 figure 6) may be acted upon by at least one bit position of the control register (element 2 figure 1) (page 5 paragraph 7) [the control register control what is executed on the processor (table 1) thus control what data does the selection circuit select for processing in the ALU].

As per claim 8, the rejection of claim 1 is incorporated and Wille further discloses:
A portable data carrier having at least one data processing device as claimed in claim 1 (Column 1 lines 6-9).

As per claim 9, the rejection of claim 1 is incorporated and Wille further discloses:
A semiconductor chip comprising at least one integrated data processing device as claimed in claim 1 (Column 1 lines 10-11).

22. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wille in view of Blount, as applied to claim 3 above, and further in view of Hooker (USPN 6832296).
As per claim 5, the rejection of claim 3 is incorporated and the combination of Wille and Blount disclose claim 3.

Neither Wille nor Blount disclose a counting register for indicating the register sets to be loaded in sequence.

However Hooker discloses a counting register (element 124 figure 1) for indicating the register sets [data in cache line] to be loaded in sequence [incrementing by cache line size each fetch (element 532 figure 1, column 10)] is assigned to the control logic circuit (element 144 figure 1) to indicate the amount of data to be fetched into the cache.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the system of Wille and Blount to include a counting register to specify the amount of data left to fetch (Hooker column 2 line 67 – column 3 line 1). By indicating the amount of data left to fetch, repeated loading of the register for controlling data transfer could be avoided (Wille column 1 line 67 – column 2 line 5).

23. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wille in view of Nemirovsky et al. (USPN 6292888, hereinafter Nemirovsky) and further in view of Hooker.

As per claim 10, Wille discloses:

i) initialization of at least one address register (element 211, 221 figure 1) by the microprocessors (element 2 figure 1) [microprocessor write value to all register, and the register 211 and 221 indicate the starting address of operands (column 3 lines 9-11, 28-31)]; (ii) starting of the calculation by assertion of at least one control bit [calculation is started by changing the bits in the control register to indicate that the operands are valid (column 4 lines 9-13); (iii) copying or loading of data beginning at the start address from

at least one in particular peripheral memory (element 4,6 figure 1) into temporary register (element 12 figure 1) [register 12 take data from the output of memory 4 (column 2 lines 53-54); (ix) starting of the calculation in the arithmetic unit (element 3 figure 1) when data is moved from temporary register (element 12 figure 1) to main register (element 14-16 figure 1) [register 12 send operands to registers 14-17 through bus 13 then input to the arithmetic unit (column 2 lines 52-58)].

Wille does not disclose the rest of the steps and that there are multiple temporary registers.

However Blount discloses a set of temporary registers (Blount AAH, ABH figure 6) connected to main register (Blount element 35 figure 6) and for storage of data for the active calculation in the ALU [the data in the register represents the input of the MAC/ALU (Blount page 11 paragraph 4)] for the purpose of sharing instruction words between adjacent processors (Blount page 11 paragraph 4).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have multiple temporary registers connected to the set of main registers in the system of Wille because Blount teaches that the multiple temporary registers enable instruction data to be shared between adjacent processor (Blount page 11 paragraph 2). Enable instruction data to be shared between adjacent processor [the microprocessor (Wille element 5 figure 1) and the arithmetic unit (Wille element 3 figure 1)] would not have to go through the memory (Wille element 6 figure 1) thus the

reduction of time need for exchanging data between the microprocessor and the arithmetic unit.

Neither Wille nor Blount discloses the rest of the steps.

However Nemirovsky discloses (v) establishing whether the set of temporary registers is complete: (v.a) if the set of temporary registers (element 4 figure 1) is complete, proceeding to method step (vi); (v.b) if the set of temporary registers (element 4 figure 1) is incomplete, proceeding to method step (iii); [the register transfer unit transfer new data to register file 4 till all data is transferred (column 7 lines 32-45)] (vi) establishing whether the arithmetic unit is active: (vi.a) if the arithmetic unit is active, proceeding to step (vi) [new register file stay in state 5 (data to be processed) till artithmetic unit is free (column 7 lines 41-50] (vi.b) if the arithmetic unit is inactive, proceeding to process new register file [when the IP is free and register file 4 is completely filled with copied data, the IP will start processing the register file 4 (column 7 lines 45-51)]. Nemirovsky's teaching enables something outside of the processor (in this case RTU) to control the register file and modify the register file's content.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to follow Nemirovsky's way to process the data transfer for registers in the combination of Wille and Blount because it enables something outside of the processor to control the register file and modify the register file's content (Nemirovsky column 2 lines 34-38). Therefore the extra entity that able to control the register file can write new

data into the inactive register at all time so that the data will be available upon the complete of a cycle in the arithmetic unit.

Neither Wille nor Blount nor Nemirovsky discloses the step from vii to xi as claimed. However Hooker discloses (vii) copying or transferal of data from the set of temporary registers (element 166 figure 1) into at least one set of main registers (element 154 figure 1) [data is written from the reponse buffer 166 into the cache 154 (column 10 lines 61-62)] (viii) decrementation of the counting register (element 124 figure 1, element 532 figure 5) (Column 10 lines 30); (x) establishing whether the counting register has been decremented to zero (element 534 figure 5) [determining whether RPC is zero that is everything need to be fetched is fetch (column 10 lines 36 –37)]: (x.a) if the counting register has been decremented to zero, proceeding to method step (xi) (element 534 figure 5); (x.b) if the counting register has not been decremented to zero, proceeding to continue fetching data from memory [the flow goes back to element 512 to continue prefetching (column 10 lines 39-40)]; (xi) termination (stop figure 5). Hooker's teaching enable specifying amount of data needs to be prefetch.
It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make use of Hooker's method to prefetch and include the necessary hardware (counting register) in the system of Wille, Blount and Nemirovsky so it can specifying amount of prefetch to be done (Hooker column 2 line 67 – column 3 line 1). Therefore the prefetching can ensure the availability of new data upon completion of a operation in the arithmetic unit.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. MacGregor et al. (USPN 4914578) discloses a system with microprocessor and an additional arithmetic unit, data to the arithmetic unit is first transfer from the memory to the temporary register, then to the unit through the main register.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Fong whose telephone number is 571-270-1409. The examiner can normally be reached on 7:00-3:30 Mon - Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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